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## **ABSTRACT OF THE DISCLOSURE**

An electrical interconnect structure on a substrate, which includes:  
a first low-k dielectric layer; a spin-on low k CMP protective layer that is  
5 covalently bonded to the first low-k dielectric layer; and a CVD deposited  
hardmask / CMP polish stop layer is provided. Electrical vias and lines  
can be formed in the first low k dielectric layer. The spin-on low k CMP  
protective layer prevents damage to the low k dielectric which can be  
created due to non-uniformity in the CMP process from center to edge or  
10 in areas of varying metal density. The thickness of the low-k CMP  
protective layer can be adjusted to accommodate larger variations in the  
CMP process without significantly impacting the effective dielectric  
constant of the structure.